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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,418	07/21/2003	Narumi Ohkawa	030882	4101

38834 7590 03/05/2007

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EXAMINER	
TRAN, NHAN T	
ART UNIT	**PAPER NUMBER**
2622	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/623,418	OHKAWA, NARUMI	
	Examiner	Art Unit	
	Nhan T. Tran	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2007 and 21 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) *3,4,6-27,29-32,34,35,37 and 38* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5,28,33 and 36* is/are rejected.

7)☒ Claim(s) *2* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Species I of Figures 1-8, claims 1, 2, 5, 28, 33 & 36 in the reply filed on 1/22/2007 is acknowledged.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statements (IDS) submitted on 12/5/2003 and 1/22/2007 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Claim Objections

4. Claim 1 is objected to because of the following informalities: claim 1 recites "the same conducting layer" which should corrected to read as -- a same conducting layer --. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 28 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 28 recites "the gate electrode" in the last line of the claim. There is insufficient antecedent basis for this limitation in the claim since there are two different gate electrodes, one is the gate electrode of the first transistor and the other is the gate electrode of the fourth transistor as required in the independent claim 1. Thus, claim 28 renders indefinite.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 33 and 36 are rejected under 35 U.S.C. 102(e) as being anticipated by Koizumi (US 7,081,607).

Regarding claims 33, Koizumi discloses an image reading method for a solid-state image sensor (Figs. 12-14) comprising: a plurality of pixel units (pixels 1 shown in

Fig. 14 and details shown in Fig. 12) arranged in a row direction and a column direction, each of the plurality of pixel units including a photoelectric converter (photodiode 3), a first transistor (Q1) for transferring a signal generated by the photoelectric converter, a second transistor (Q3) for amplifying the signal, a third transistor (Q2) for resetting an input terminal of the second transistor, and a fourth transistor (Q4) for reading the signal outputted by the second transistor; a plurality of first signal lines (signal lines 67) extended in the row direction, each of the first signal lines being connected to gate electrodes of the first transistors (Q1) of the pixel units arranged in the row direction; and a plurality of second signal lines (also shared signal lines 67) extended in the row direction, each of the second signal lines being connected to gate electrodes of the fourth transistors (Q4) of the pixel units arranged in the row direction, the first signal line connected to the gate electrodes of the first transistors (Q1) of the pixel units of an n^{th} row (which is $n-1^{th}$ row in Fig. 12), and the second signal line connected to the gate electrodes of the fourth transistors (Q4) of the pixel units of an $n+1^{th}$ row (which is n^{th} row in Fig. 12) being formed of **a common signal line** (common line 67; see col. 10, lines 49-61), the method comprising the steps of:

globally resetting (by vertical scanning 101 shown in Fig. 14 that sends reset control pulses ØRn) the photoelectric converters and the second transistors in all the rows (see col. 10, line 49 – col. 11, line 42 and it should be noted that all rows are globally reset in sequential manner within one frame period);

after a period of a photo detection time (an accumulation period), globally transferring charges from the photoelectric converters (photodiode 3) to the gate

terminals of the second transistors (Q3) via the first transistors (Q1) in all the rows; reading signals and reading reset voltages in each of the rows (see col. 10, line 62 – col. 11, line 42 and it should be also noted that signal charges from all rows are globally transferred within one frame period).

Regarding claim 36, as shown in the timing chart of Fig. 13 of Koizumi, the step of resetting the photoelectric converter and the second transistors (indicated by active high of ØR1 in Fig. 13) and the step of transferring charges (indicated by active high of ØS2) to the gate terminals of the second transistors are performed with signal read lines shut off from peripheral circuits (indicated by active low of Ø22 and Ø24 of peripheral circuits; it is noted that details of peripheral circuits are shown in Fig. 4; see col. 10, line 62 – col. 11, line 42).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 5 & 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koizumi (US 7,081,607 B1) in view of Guidash et al. (US 6,466,266 B1).

Regarding claim 1, Koizumi discloses a solid-state image sensor (Figs. 12 & 14) comprising:

a plurality of pixel units (pixel units 1 shown in Fig. 14 and details shown in Fig. 12) arranged in a row direction and a column direction, each of the plurality of pixel units including a photoelectric converter (photodiode 3), a first transistor (Q1) for transferring a signal generated by the photoelectric converter, a second transistor (Q3) for amplifying the signal, a third transistor (Q2) for resetting an input terminal of the second transistor, and a fourth transistor (Q4) for reading the signal outputted by the second transistor (see Fig. 12 and col. 10, lines 49-61);

a plurality of first signal lines (signal lines 67) extended in the row direction, each of the first signal lines being connected to gate electrodes of the first transistors (Q1) of the pixel units arranged in the row direction (see Fig. 12);

a plurality of second signal lines (also shared signal lines 67) extended in the row direction, each of the second signal lines being connected to gate electrodes of the fourth transistors (Q4) of the pixel units arranged in the row direction, the first signal line connected to the gate electrodes of the first transistors of the pixel units of an n^{th} row (which is $n\text{-}1^{th}$ row in Fig. 12 of Koizumi), and the second signal line connected to the gate electrodes of the fourth transistors of the pixel units of an $n+1^{th}$ row (which is n^{th} row in Fig. 12 of Koizumi) being formed of **a common signal line** (common line 67) (see col. 10, lines 49-61), and in each pairs of the pixel units of the n^{th} row (which is $n\text{-}1^{th}$ row in Fig. 12) and the $n+1^{th}$ row (which is n^{th} row in Fig. 12) corresponding to each other, the gate electrode of the first transistor (Q1(n-1)) of the pixel unit of the n^{th} row

and the gate electrode of the fourth transistor (Q4(n)) of the pixel unit of $n+1^{th}$ row are being formed by one continuous pattern of a conducting material (see Fig. 12).

Although Koizumi teaches the common signal line (67) as a continuous conducting material which is connected to the gate of transistor Q1(n-1) and the gate of transistor Q4(n) as shown in Fig. 12, Koizumi does not fairly teach that the continuous pattern of the conducting material is on a same conducting **layer**.

Guidash teaches a practice for layout of conducting layers for an image sensor in which a common line (TG BUS 23 shown in Fig. 4) connecting to a gate of a transistor of one row and a gate of another transistor of an adjacent row is continuously formed within a same conducting layer (see Guidash, Fig. 4; col. 3, lines 49-65 and col. 4, lines 30-33). Guidash teaches that such layout structure reduces a total of number of signal lines and line contact areas in each pixel, thereby improving fill factor and sensitivity of the image sensor (Guidash, col. 1, line 65 – col. 2, line 5).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Koizumi and Guidash to arrive at the Applicant's claimed invention so as to reduce a total of number of signal lines and line contact areas in each pixel, thereby improving fill factor and sensitivity of the image sensor as taught by Guidash above.

Regarding claim 5, Koizumi also discloses that a solid-state image sensor according to claim 1, wherein the photoelectric converter and the first transistor are adjacent to each other in the row direction (see Fig. 12 of Koizumi), the second

transistor (Q3) and the third transistor (Q3) are adjacent to each other in the column direction (Fig. 12 of Koizumi), and the gate electrode of the first transistor (Q1 at line 16) and the gate electrode of the fourth transistor (Q4 at line 17) are extended in the column direction (see Fig. 12 of Koizumi).

Regarding claim 28 *(note that this claim is rejected based on best understood in view of the 35 USC 112 2nd paragraph rejection above)*, Koizumi in view of Guidash discloses a contact hole (contact hole at FD shown in Fig. 4 of Guidash) opened onto a source region of the third transistor (which is the source of the reset transistor RG), and a contact hole (contact hole of RSG) opened onto a source region of the fourth transistor (select transistor RSG) are formed by self-alignment with the gate electrode (see Guidash, Fig. 4).

Allowable Subject Matter

8. Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

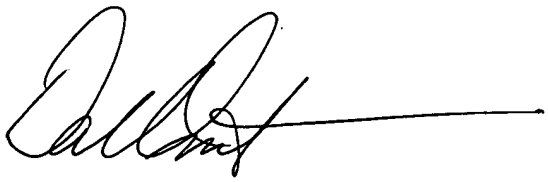
Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

NHAN T. TRAN
Patent Examiner



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